In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Currently amended) A delay locked loop comprising a line of n delay cells (R1, R2, ..., Rn) mounted in series from a delay cell of rank 1 to a delay cell of rank n, n being an integer greater than or equal to 2, each delay cell outputting a delayed signal, the line of delay cells having an input which is an input of the delay cell of rank 1 and which is connected to a first input of a phase/frequency detector, wherein said delay locked loop comprises control means including a sigma delta modulator (6) and having n inputs and an output, each input of the control means being connected to an output of a different delay cell of the line of delay cells and the output of the control means being connected to a second input of said phase/frequency detector, said control means selecting at each clock signal (H), on the basis of a control information (I), one of the ~~which~~ delayed signals for applying ~~signal among the different delayed signals is applied~~ to said second input of said phase/frequency detector, the number of delay cells seen by the phase/frequency detector being able to change at each tick of the clock signal (H).

2. (Previously presented) Delay locked loop according to claim 1, wherein the control means comprise multiplexing means (4) with n inputs and one output,

3. (Currently amended) ~~Phased~~ Delay locked loop according to claim 2, wherein the multiplexing means (4) comprise a multiplexer (5) and ~~a~~ the sigma delta modulator (6) with a clock input on which said clock signal (H) is applied and a signal input on which said control information (I) is applied, the sigma delta modulator (6) outputting a digital control signal applied to the multiplexer (5).

4. (Currently amended) A delay locked loop comprising a line of n delay cells (R1, R2, ..., Rn) mounted in series from a delay cell of rank 1 to a delay cell of rank n, n being an integer greater than or equal to 2, each delay cell outputting a delayed signal, the line of delay cells having an input which is an input of the delay cell of rank 1 and which is connected to a first

input of a phase/frequency detector, wherein said delay locked loop comprises control means having n inputs and an output, each input of the control means being connected to an output of a different delay cell of the line of delay cells and the output of the control means being connected to a second input of said phase/frequency detector, said control means selecting at each clock signal (H), on the basis of a control information (I), one of the delayed signals for applying to said second input of said phase/frequency detector, the number of delay cells seen by the phase/frequency detector being able to change at each tick of the clock signal (H)~~Delay-locked loop according to claim 1~~, wherein the control means comprise a first set of n switches Iqi (i = 1, 2, ..., n), a second set of n switches Ipi (i = 1, 2, ..., n) and a control circuit (7) with a clock input on which said clock signal (H) is applied and a control input on which said control information (I) is applied, the switch Ipi (i=1, 2, ..., n) being placed at the output from the delay cell of rank I (i=1, 2, ..., n) and the switch Iqi being placed in parallel with an assembly formed by the delay cell of rank i and the switch Ipi, switches Ipi and Iqi being controlled by control signals pi and qi respectively output from the control circuit (7).

5. (Previously presented) Delay locked loop according to claim 4, wherein additional switches and switchable loads are placed at the input and output of the different delay cells (R1, R2, ..., Rn) such that the total number of switches used in the loop during operation of the loop is always the same, and each delay cell always sees the same load on its input and on its output.

6. (Canceled)

7. (Previously presented) Delay locked loop according to claim 1, wherein the control information (I) is a fractional value p/q such that the output from the delay line is composed of the output from the rank n-1 delay cell for p ticks of the clock signal and the output from the rank n delay cell during q ticks of the clock signal, where p and q are two integer numbers and q is greater than p, and the value of the delay of a delay cell is given by the relation:

$$\Delta t = q\,T/(qn-p),$$

where T is the period of a signal applied to the input of the delay line.

8. (Previously presented) Delay locked loop according to claim 1, wherein the clock signal (H) is a same signal as a clock signal applied to the first input of the phase/frequency detector (1), except for a delay.

9. (Previously presented) Delay locked loop according to claim 1, wherein the clock signal (H) is a signal with a period less than the period of a signal applied to the first input of the phase/frequency detector (1).

10. (Previously presented) Delay locked loop according to claim 1, wherein it comprises means (8, 9, 10) to select a number of delay cells such that the loop will not get locked, during a loop latching phase.

11. (Previously presented) Delay locked loop according to claim 10, wherein the means (8, 9, 10) provided to select a number of delay cells to prevent the loop from getting locked, during a loop latching phase, comprise a convergence analysis device (8), a switch (9) and a processing circuit (10), the input to the convergence analysis device (8) being connected to the output from the phase/frequency detector (1), the switch (9) being controlled such that the output from the convergence device (8) is connected to the input to the processing circuit (10), the output from the processing circuit (10) being connected to a control input of the control means (4, 7).

12. (Previously presented) Delay locked loop according to claim 10, characterised in that it comprises means (10) of memorising the selected number of delay cells.

13. (New) Delay locked loop according to claim 4, wherein the control information (I) is a fractional value p/q such that the output from the delay line is composed of the output from the rank n-1 delay cell for p ticks of the clock signal and the output from the rank n delay cell during q ticks of the clock signal, where p and q are two integer numbers and q is greater than p, and the value of the delay of a delay cell is given by the relation:

$$\Delta t = q\ T/(qn-p),$$

where T is the period of a signal applied to the input of the delay line.

14. (New) Delay locked loop according to claim 4, wherein the clock signal (H) is a same signal as a clock signal applied to the first input of the phase/frequency detector (1), except for a delay.

15. (New) Delay locked loop according to claim 4, wherein the clock signal (H) is a signal with a period less than the period of a signal applied to the first input of the phase/frequency detector (1).

16. (New) Delay locked loop according to claim 4, wherein it comprises means (8, 9, 10) to select a number of delay cells such that the loop will not get locked, during a loop latching phase.